A 2.4GHz Dual-Modulus Divide-by-127/128 Prescaler in 0.35μm CMOS Technology

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Abstract –High speed design solution for high divide-by-value dual modulus prescaler remains a challenge in designing high frequency synthesizers in CMOS technology. This paper presents a dual-modulus divide-by-127/128 prescaler implemented in 0.35μm CMOS technology operating at 2.4GHz frequency. Unlike the conventional topologies, this design is based on a novel way of dual-modulus division using four transmission gates in critical path. It consumes 4.8mW power from a 3V supply. Measurement results are provided.

I. INTRODUCTION

Frequency synthesizers have wide area of applications including modern wireless communication systems. In such applications, CMOS design of Phase Locked Loop (PLL) based frequency synthesizers used to generate very high frequency using a low reference frequency is challenging. It has stringent requirements of high speed and high divide-by-value on Dual Modulus Prescaler (DMP) which is one of its critical building blocks.

Dual modulus prescaler usually comprises of a synchronous dual modulus counter and an asynchronous counter. High speed, high divide-by-value and low power dissipation are the challenging design requirements of a DMP. The delay of critical path and the speed of D flip-flop (DFF) in synchronous counter limit its speed particularly at high divide-by-value. Conventionally high divide-by-value is, in general, achieved by adding flip-flops in asynchronous counter at the cost of additional load resulting in degraded speed. Several attempts have been made to improve the performance of DFF[1-4] and to improve the speed by minimizing delay in critical path[5,6]. The conventional DMP designs reported in [1-6] show their limitations to operate at high frequencies such as 2.4GHz for a high divide-by-value such as 127/128. The limiting factors for their performance on speed and divide-by-value include critical path delay due to logic gates used for mode selection.

In this paper, an alternative topology for the CMOS design of a low power, high speed and high divide-by-value DMP is presented. It is based on the principle of mode selection using transmission gates in the critical path.

The circuit topology and principle of operation of the proposed design is described in section II. Section III provides design implementation and test results followed by conclusions in last section.

II. CIRCUIT TOPOLOGY AND PRINCIPLE OF OPERATION

Fig. 1 shows a widely used CMOS topology for high-speed and high divide-by-value dual modulus prescaler. It is consisting of dual modulus divide-by- 4/5 synchronous counter and divide-by-32 asynchronous counter. The critical path (i.e. from Q1 to D1 via asynchronous counter, combinational circuit, NAND2, DFF#3 and NAND1) delay is primarily due to the two nand gates, one D flip-flop and the combinational circuit.

The circuit based on a novel way of generating mode control logic using transmission gates in critical path (i.e. qb2 to d2 via TG3 and TG2) is presented in Fig. 2. Table 1 (a) and (b) represents its states of transition during the mode of division by 4 and 3 respectively. The circuit operation can be illustrated as follow:

For divide-by-4 case: Q1Q2 state cycles as 00 to 10 to 11 to 01 to 00 and so on. For divide-by-3 case: it skips state 01 and state changes directly from 11 to 00. In other words, for divide-by-3 case, whenever Q2=1, it needs to be reset to 0. Here, this is achieved by generating control signal S from mode control using transmission gate TG3 and TG4. When TG1 is ON (TG2 is OFF), DFF1 and DFF2 function as divide-by-4 counter else as divide-by-3.

When mode control signal is put in divide by 4 mode, TG3 is put in OFF state and TG4 is made ON. It switches off TG2 and on TG1. This allows Q2=D2=Q1 and circuit operates in divide-by-4 mode. Whereas, when mode control is in divide by3 mode, TG4 is in OFF state and TG3 is turned ON. This turns on TG2 and off TG1. This resets Q2=D2=0 resulting in the divide-by-3 mode operation of the circuit. It may, however, be noted here that all transmission gates and the control logic need to be properly designed such that the above conditions are met to provide the mode selection operation.

The schematic for a 127/128 dual-mode prescaler is shown in Fig. 3. It is comprised of a synchronous dual modulus divide-by-3 / 4 counter as described above and an asynchronous divide-by-32 counter. The mode control level and output of divide-by-32 counter control TG3 and TG4. As a consequence, the whole circuit functions as divide-

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by-127/128. For high frequency operation requirement, the high speed DFFs are used in the synchronous counter and as the asynchronous counter operates at low frequency, True Single Phase Clock (TSPC) TFFs are used which consume low power.

Table 1: (a) State table for divide by 4 counter

State	Present state Q1Q2	Next state Q1' Q2'
1	0 0	1 0
2	1 0	1 1
3	1 1	0 1
4	0 1	0 0

Table 1: (b) State table for divide by 3 counter

State	Present state Q1Q2	Next state Q1' Q2'
1	0 0	1 0
2	1 0	1 1
3	1 1	0 1

III. DESIGN IMPLEMENTATON AND TEST RESULTS

The circuit is designed using Hspice and Cadence design environment is used for layout development. Circuit layout is included inside a 24 pin chip having a total silicon area of 800µm x 800µm only. The device is fabricated using standard CMOS 0.35 µm process. It is packaged using 24-pin Quad Flat Package and mounted on Printed Circuit Board designed with 50 Ohm microstrip line for RF frequencies. Equipment used for testing includes Signal Generator HP 83712B, Spectrum Analyzer HP8593E, Oscilloscope Tektronix 2465B and Agilent E3646A DC Power Supply. Fig. 4 to Fig. 7 show prescaler output spectra and waveforms, captured using digital camera, at divide-by-127 and divide-by-128 operations while it is operated at 3V supply with an input frequency of 2.4GHz. Test results for input power sensitivity level versus input frequency are provided in Fig. 8 and Fig. 9 for two samples while operated at divide-by-127 and divide-by-128 respectively. Input sensitivity and output power levels can further be improved using I/O buffers in the design. Die microphotograph is depicted in Fig. 10. Table 2 summarizes test results. The die containing six test structures of similar complexity connected to a common supply consumes 36mW at 3V supply. However, Hspice simulation shows prescaler consumes 4.8mW only.

III. CONCLUSION

A high speed, low power and high divide-by-value dual modulus prescaler is presented. A novel approach, unlike to conventional ways, of mode selection using four transmission gates in the critical path is demonstrated. Avoiding the use of flip flop and logic gates in the critical path provides additional advantages of low power and low load to Voltage Controlled Oscillator, generally integrated with prescaler, besides minimizing the design complexity. Design is fabricated using CMOS 0.35µm process and test results are provided for its divide-by-127/128 operation at 2.4GHz/3V. This topology can reduce the challenges faced in designing high frequency synthesizers for communication systems.

Table 2: Measurements Summary at 3V Supply

Parameter	**Performance**
Division Ratio	127 and 128
Max. operating frequency	2.4GHz @ divide-by-127 operation
Max. operating frequency	2.5GHz @ divide-by-128 operation
Output Power (2.4GHz input frequency)	5dBm
Prescaler Power Consumption	4.8mW @ 3V (Simulated)
Die Power Consumption	36mW @3V 27mW@2.7V
Operating Voltage	2.7V-3.3V
Sensitivity level	15dBm @2.4GHz
Die area	0.8 x 0.8 mm^2
Technology	CMOS 0.35µm CSM

ACKNOWLEDGEMENT

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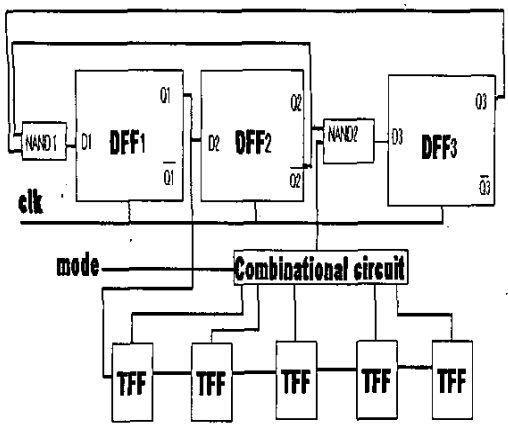

Fig.1: A conventional dual modulus prescaler

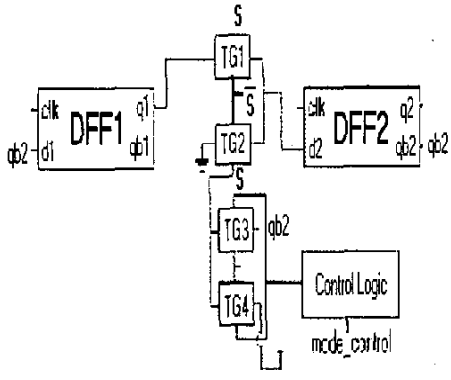

Fig. 2: Synchronous divide-by-3 / 4 counter.

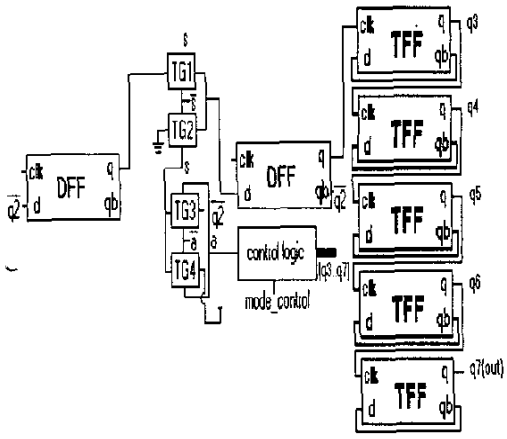

Fig. 3: Divide-by-127/128 prescaler

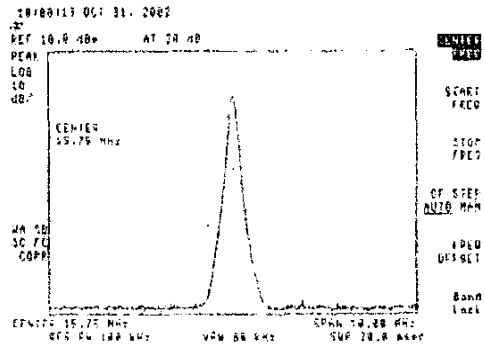

Fig.4: Output spectrum at divide-by-127 operation (Input Frequency 2.4GHz)

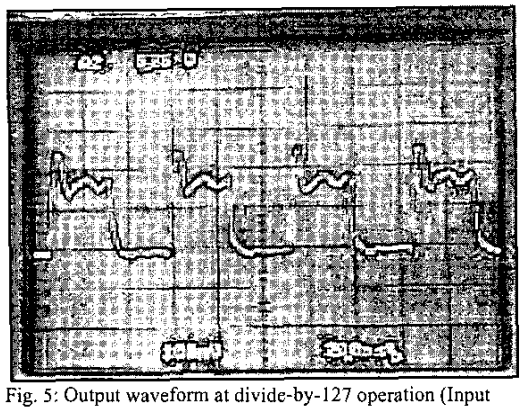

Fig. 5: Output waveform at divide-by-127 operation (Input frequency 2.4GHz)

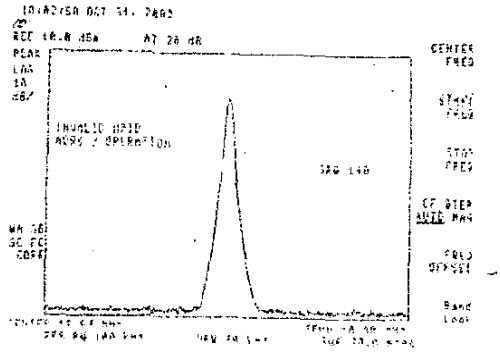

Fig.6: Output spectrum at divide-by-128 operation (Input Frequency 2.4GHz)

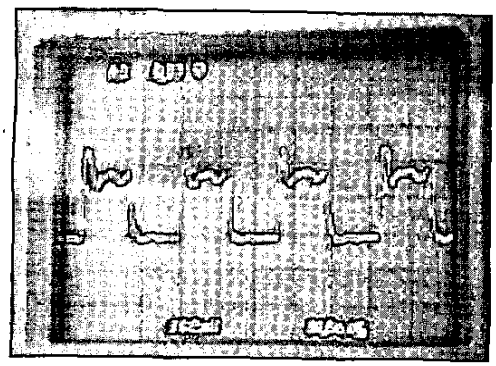

Fig. 7: Output waveform at divide-by-128 operation (Input frequency 2.4GHz)

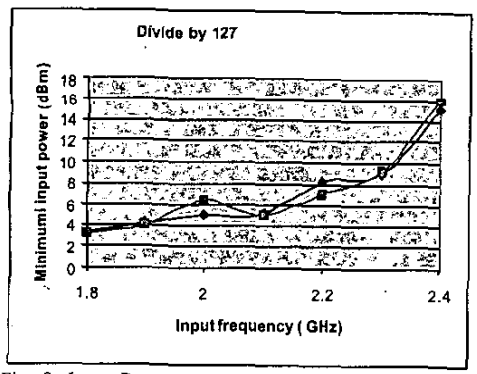

Fig. 8: Input Power versus Frequency at Divide-by-127 operation for two dies

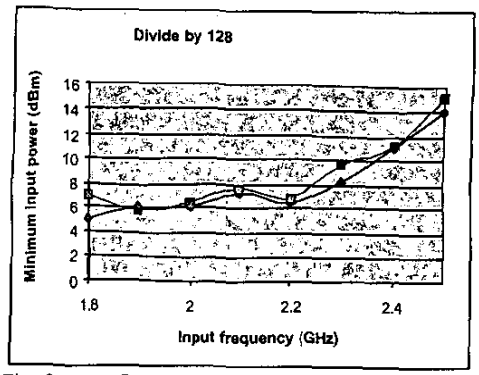

Fig. 9: Input Power versus Frequency at Divide-by-128 operation for two dies

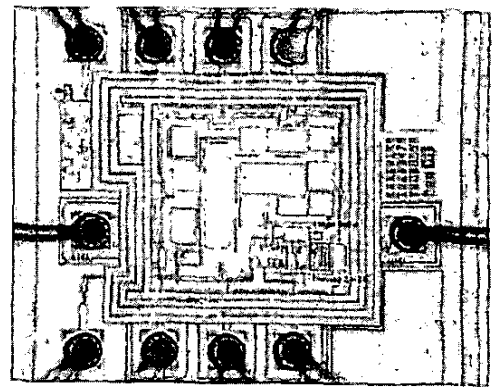

Fig. 10: Die Photograph